

AMENDMENTS TO THE CLAIMS

Claims 1-19 (Canceled)

Claim 20 (Newly Added): A method for fabricating a semiconductor memory element arrangement, comprising the steps of:

forming a first electrically insulating layer on a substrate;

forming a layer system, including a floating gate and a multiple tunnel barrier arrangement formed on the floating gate, on the first electrically insulating layer;

forming a first trench structure in the layer system, the first trench structure having first trenches arranged parallel to one another and extending as far as the first electrically insulating layer;

forming a second trench structure in the layer system, the second trench structure having second trenches arranged parallel to one another and extending as far as the first electrically insulating layer, the second trenches being arranged perpendicular to the first trenches;

forming, in the first and second trench structures, a first gate electrode adjacent to the floating gate through which first gate electrode electrical charge can be fed or can be dissipated from; and

forming, in the first and second trench structures, a second gate electrode adjacent to the tunnel barrier arrangement, wherein through the second gate electrode an electrical charge transmission of the multiple tunnel barrier arrangement can be controlled.

Claim 38 (Newly Added): A semiconductor memory element arrangement, in which a plurality of semiconductor memory elements are arranged in a matrix-like manner in a plurality of rows and columns, each semiconductor memory element comprising:

- an electrically insulating layer formed on a substrate;

- a layer system formed on the electrically insulating layer, wherein the layer system includes a floating gate and a tunnel barrier arrangement formed on the floating gate and forming a multiple tunnel barrier;

- a first trench structure formed in the layer system and having first trenches arranged parallel to one another and extending as far as the electrically insulating layer;

- a second trench structure formed in the layer system and having second trenches arranged parallel to one another and perpendicular to the first trenches and extending as far as the electrically insulating layer;

- a first gate electrode formed in the first and second trench structures and adjacent to the floating gate, wherein the first gate electrode determines the charge carriers stored in the floating gate; and

- a second gate electrode formed in the first and second trench structures and adjacent to the tunnel barrier arrangement, wherein via the second gate electrode the charge transmission of the tunnel barrier arrangement may be controlled.